For example, claim 1 specifies "storing address information from the layer 2 packet, including the host identifier, in a selected one of a plurality of address tables within the switching module based on the corresponding subnetwork identifier, each of the address tables configured for storing the host identifiers of respective transmitting nodes of a corresponding one of the subnetworks".

Claim 10 specifies "selecting one of a plurality of address tables within the switching module based on the corresponding subnetwork identifier, each of the address tables configured for storing the host identifiers of respective transmitting nodes of a corresponding one of the subnetworks".

Claim 17 specifies "a switching module ... including a plurality of address tables for storing the layer 3 switching information for the respective subnetworks, the switching module accessing a selected one of the address tables based on the corresponding subnetwork identifer...."

Hence, the integrated network switch utilizes a (i.e., at least one) switching module, where the one switching module includes multiple address tables for storing layer 3 switching information for respective subnetworks. Hence, search times for layer 3 switching information can be dramatically reduced by providing a plurality of address tables within a single switching module and that can be independently accessed by the switching module on a per-subnetwork basis.

Further, use of multiple address tables for respective subnetworks within a single switching module optimizes layer 3 switching operations while maintaining a low cost, economical architecture based on a centralized switching module that can be optimized to minimize area on the integrated circuit.

These and other features are neither disclosed nor suggested in the applied prior art.

As admitted in the Official Action, Vig does not disclose the "plurality of address tables within switching [sic] module based on corresponding [sic] subnetwork identifier, each of the address tables configured for storing the host identifiers of respective transmitting nodes of a corresponding one of the subnetworks.

Moreover, Vig is not merely silent as to this claimed feature, but teaches away from this claimed feature by disclosing that a single subnet may be served by multiple switch ports, hence Vig uses a single table for all subnet-to-port mapping. For example, Vig specifies at col. 3, lines 12-16: "[t]he switch builds a subnet to port mapping table based on packets received from each source host and selectively forwards the multicast packet to all ports on which the destination subnet is active."

Further, Vig teaches at col. 8, lines 8-12 that the CPU performs centralized processing of the layer 3 information, and column 8, line 51 to column 9, line 2, specifies that Vig relies on a single table for all subnet-to-port mapping.

Hence, Vig teaches use of a centralized CPU and a single table for subnet-to-port mapping.

The teaching of Vig is significant because the Official Action fails to establish why one having skill in the art would have been motivated to modify Vig to add the teachings of Kadambi. The Official Action asserts that "one of ordinary skill in the art would be motivated to do this for efficient address mapping." However, as demonstrated below, this assertion is without foundation and inconsistent with the teachings of the references. Further, Applicant objects to this supposed motivation, since the Examiner is using the claimed invention as a template to combine the references.

Kadambi illustrates in Figure 2 that each Ethernet Port Interface Controller (EPIC) 20 supports 8 fast ethernet ports 13 (col. 5, lines 40-41), and that each EPIC 20 is associated with (i.e.,

assigned) a corresponding address resolution logic (ARL) and layer three table (ARL/L3) 21, rules table 22, and VLAN table 23 (see col. 5, lines 30-37 and 54-61). Note that only the ARL/L3 table 21 stores layer 3 information.

Kadambi further stresses that each EPIC 20 operates individually and independently of other EPICs (see col. 5, lines 1-9; col. 10, 56-63). Hence, each EPIC 20 has an input port 24 with a L2/L3 engine 143 (see Fig. 14) and an ingress submodule 14 (see Fig. 8): only the ARL/ L3 table 21 stores layer three information. (see col. 11, lines 3-8 and 20-28; col 18, lines 41-45, and column 27 in its entirety).

Hence, Kadambi teaches that each EPIC 20a, 20b, etc. performs its own corresponding layer 2/layer 3/ processing by accessing its own corresponding table 21. Consequently Kadambi teaches multiple switching modules 143 that are distributed among the respective EPICs 20 to provide parallel and independent processing. This parallel processing, however, is substantially costly in terms of duplicating all tables and switching modules 143 in all port interface controllers 20, and Gigabit Port Interface Controllers 30. Moreover, Kadambi neither discloses nor suggests storing host identifiers, as claimed.

Contrary to the assertions of the Official Action, one having ordinary skill in the art would not have been motivated to modify Vig to include the teachings of Kadambi, since the multiple tables described by Kadambi would be inconsistent with the single table of Vig.

Hence, one having skill in the art would not have been motivated to add the teachings of Kadambi to Vig. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Fritch, 23 USPQ2d 1780, 1783-84 (Fed. Cir. 1992). "Teachings of

references can be combined only if there is some suggestion or incentive to do so." In re Fine, 5 USPQ2d 1596,1600 (Fed. Cir. 1988) (quoting ACS Hosp. Sys. v. Montefiore Hosp., 221 USPQ 929, 933 (Fed. Cir. 1984)) (emphasis in original).

In this case, no such motivation has been demonstrated. In fact, Applicant strenuously objects to the Examiner's use of the claimed invention to combine the references: there is no identification that the address mapping of Vig or Kadambi is inefficient, or that combination thereof would in any way improve efficiency. "It is impermissible to use the claimed invention as an instruction manual or 'template' to piece together the teachings of the prior art so that the claimed invention is rendered obvious." In re Fritch, 23 USPQ2d 1780, 1784 (Fed. Cir. 1992).

Assuming one skilled in the art combined Vig and Kadambi, the resulting hypothetical combination still would neither disclose nor suggest the claimed feature that that the switching module includes a plurality of address tables for storing the layer 3 switching information for the respective subnetworks, where each address table is configured for storing host identifiers for a corresponding subnetwork. Rather, Kadambi requires that each Port Interface Controller (e.g., EPIC 20, GPIC 30) have its own corresponding ARL/L3 table 21 and its own switching module 143 in order to provide complete and independent parallel processing for each Port Interface. As described above, this arrangement is extremely costly due to the duplication of all modules in each port 20 (e.g., 20a, 20b, 20c, etc.) and 30. Moreover, each ARL/L3 table 21 would only store the subnet address for a destination subnet: there is no disclosure or suggestion that the ARL/L3 table 21 would store the host identifiers, as claimed.

Hence, the hypothetical combination would require multiple switching modules having respective tables.

The independent claims, however specify a switching module includes a plurality of address tables.

More fundamentally, however, the hypothetical combination still neither discloses nor suggests that each address table is configured for storing host identifiers for a corresponding subnetwork, as claimed. In fact, Kadambi teaches that multiple subnetworks may be identified in a single address table 21 to enable the ingress port 24 to identify a destination subnet match. (See col. 26, lines 61-68, col. 27, lines 22-23 and 37-41; col 28, lines 13-16). However, there is no disclosure or suggestion of storing the host identifiers, as claimed, especially in tables on a per-subnetwork basis.

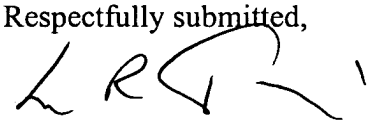
Hence, the §103 rejection of independent claims 1, 10, and 17 should be withdrawn.

Applicant further traverses the rejection of claims 3-4, 12-13, 21-22. Vig discloses that a single subnet may be served by multiple switch ports. Further, Vig uses a single table for all subnet-to-port mapping (see, e.g., col. 3, lines 12-16; col. 8, line 51 to col.9, line 2). Kadambi teaches that each port interface controller has its own corresponding set of tables and switching module, and that the layer 3 tables will include multiple subnet addresses for destination subnets. Neither Vig nor Kadambi disclose, singly or in combination, that each network switch port is connected to a corresponding subnetwork, let alone that each address table is assigned to a corresponding one network switch port, as claimed. Hence, these claims are further patentable over Vig and Kadambi.

In view of the above, it is believed this application is and condition for allowance, and such a Notice is respectfully solicited.

To the extent necessary, Applicant petitions for an extension of time under 37 C.F.R. 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including any missing or insufficient fees under 37 C.F.R. 1.17(a), to Deposit Account No. 50-0687, under Order No. 95-309, and please credit any excess fees to such deposit account.

Respectfully submitted,



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Date: Decenber 11, 2003